Features

- 4,194,304 word by 16 bit organization
- Single 3.3 ± 0.3V power supply
- Extended Data Out (Hyper Page Mode)
- $\overline{CAS}$ before $\overline{RAS}$ Refresh
  - 4096 cycles/retention Time
- $\overline{RAS}$ only Refresh
  - 4096 cycles/Retention Time
- 64ms Standard Power (SP) Retention Time
- 256ms Low Power (LP) Retention Time
- Hidden Refresh
- Self Refresh (400 µA) - LP Version Only
- Read-Modify-Write
- Dual $\overline{CAS}$ Byte Read/Write
- Performance:

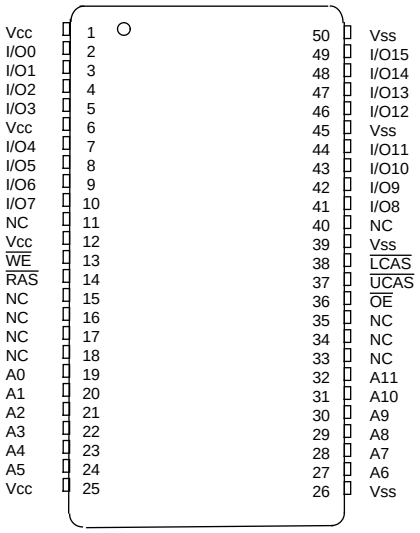
		-50	-60
t_{RAC}	$\overline{RAS}$ Access Time	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	13ns	15ns
t_{AA}	Column Address Access Time	25ns	30ns
t_{RC}	Cycle Time	84ns	104ns
t_{HPC}	Hyper Page Mode Cycle Time	20ns	25ns

- Max. Power Dissipation (-50)
  - Active: 414mW
  - Standby (SP LVCMOS): 3.6mW
  - Standby (LP LVCMOS): 0.72mW
- Package: TSOP-50 (400milx825mil)

Description

The IBM0165165B/P is a dynamic RAM organized 4,194,304 words by 16 bits. This device is fabricated in IBM's most advanced CMOS silicon gate process technology. The circuit and process design allow this DRAM to achieve high performance and low power dissipation. The IBM0165165B/P operates with a single 3.3 ± 0.3V power supply, and interfaces directly with either LVTTL or LVCMOS levels. The 22 addresses required to access any bit of data are multiplexed (12 are strobed with $\overline{RAS}$, 10 are strobed with $\overline{CAS}$). They are packaged in a 50 pin plastic TSOP type II (400mil×825mil). The IBM0165165P parts are low power devices supporting Self Refresh and a 256ms retention time.

Pin Assignments (Top View)



Pin Description

$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$ / $\overline{UCAS}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A11	Address Inputs
$\overline{OE}$	Output Enable
I/O0 - I/O15	Data Input/output
V_{CC}	Power (+3.3V)
V_{SS}	Ground

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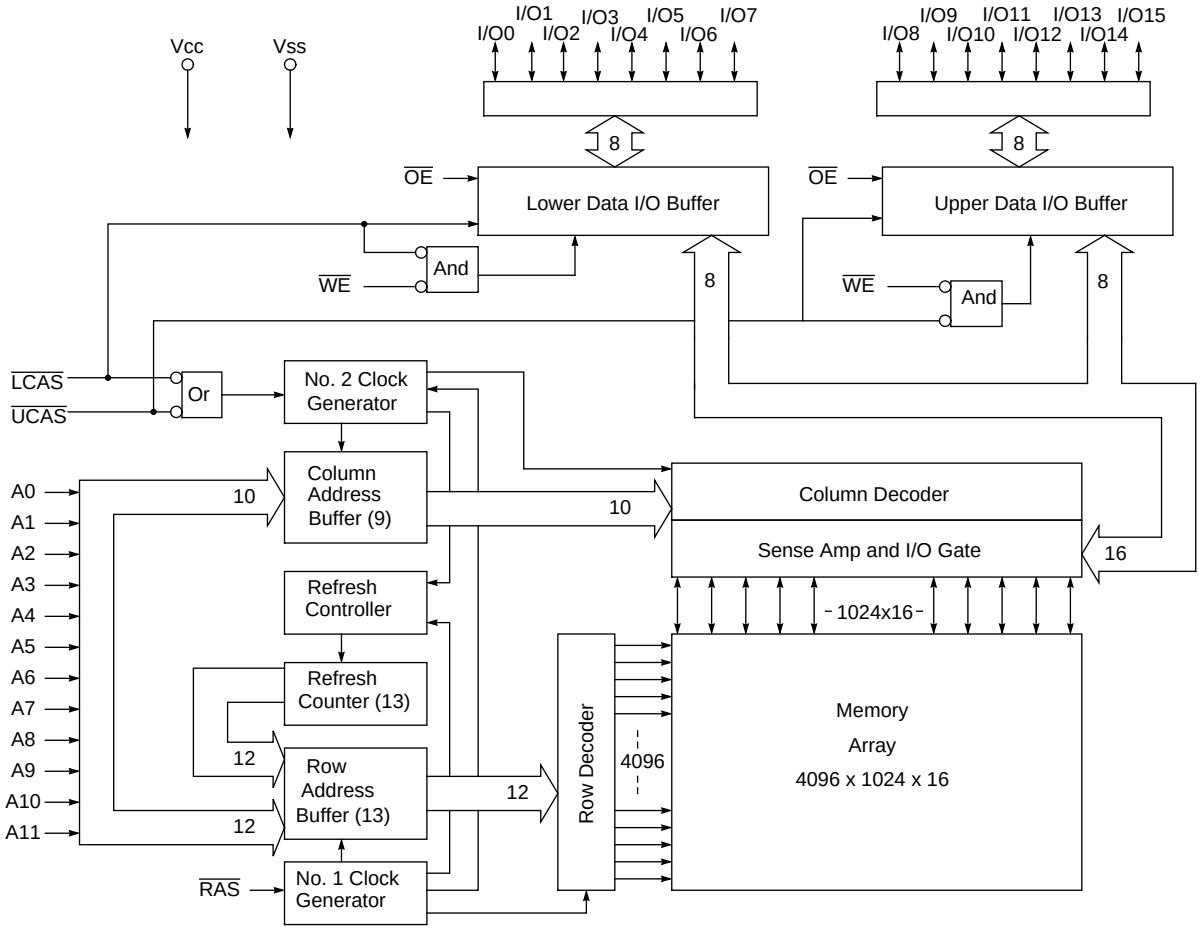
Ordering Information

Part Number	Power	Self Refresh	Power Supply	Speed	Package	Notes
IBM0165165BT3C-50	SP	No	3.3V	50ns	400mil TSOP 50	1
IBM0165165BT3C-60	SP	No	3.3V	60ns	400mil TSOP 50	1
IBM0165165PT3C-50	LP	Yes	3.3V	50ns	400mil TSOP 50	1
IBM0165165PT3C-60	LP	Yes	3.3V	60ns	400mil TSOP 50	1

1. SP = Standard Power version (IBM0165165B); LP = Low Power version (IBM0165165P)

Block Diagram



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Truth Table

Function		$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	I/O0 - I/O15
Standby		H	H→X	H→X	X	X	X	X	High Impedance
Read: Word		L	L	L	H	L	Row	Col	Data Out
Read: Lower Byte		L	L	H	H	L	Row	Col	Lower Byte: Data Out Upper Byte: High-Z
Read: Upper Byte		L	H	L	H	L	Row	Col	Lower Byte: High-Z Upper Byte: Data Out
Write: Word Early-Write		L	L	L	L	X	Row	Col	Data In
Write: Lower Byte Early-Write		L	L	H	L	X	Row	Col	Lower Byte: Data In Upper Byte: High-Z
Write: Upper Byte Early-Write		L	H	L	L	X	Row	Col	Lower Byte: High-Z Upper Byte: Data In
Read-Modify-Write		L	L	L	H→L	L→H	Row	Col	Data Out, Data In
EDO (Hyper Page) Mode Read	1st Cycle	L	H→L	H→L	H	L	Row	Col	Data Out
	2nd Cycle	L	H→L	H→L	H	L	N/A	Col	Data Out
EDO (Hyper Page) Mode Write	1st Cycle	L	H→L	H→L	L	X	Row	Col	Data In
	2nd Cycle	L	H→L	H→L	L	X	N/A	Col	Data In
EDO (Hyper Page) Mode Read-Modify-Write	1st Cycle	L	H→L	H→L	H→L	L→H	Row	Col	Data Out, Data In
	2nd Cycle	L	H→L	H→L	H→L	L→H	N/A	Col	Data Out, Data In
$\overline{RAS}$-Only Refresh		L	H	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	L	H	X	X	N/A	High Impedance
Hidden Refresh	Read	L→H→L	L	L	H	L	Row	Col	Data Out
	Write	L→H→L	L	L	H	X	Row	Col	Data In
Self Refresh (LP version only)		H→L	L	L	H	X	X	X	High Impedance

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Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 4.6	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC}+0.5, 4.6)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC}+0.5, 4.6)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	°C	1
P_D	Power Dissipation	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A=0 to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.3	V	1,2
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1,2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 2.0V for pulse widths of ≤ 4.0ns with 3.3 Volt. V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns with 3.3 Volt. Pulse widths measured at 50% points with amplitude measured peak to DC reference

Capacitance (T_A=0 to +70°C, V_{CC}=3.3 ± 0.3V, f=1MHz)

Symbol	Parameter	Min.	Max.	Units	Notes
C_{I1}	Input Capacitance (A0 - A11)	—	5	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$)	—	7	pF	
C_{I3}	Data I/O Capacitance (I/O0 - I/15)	—	7	pF	

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DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter		Min.	Max.	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-50	—	140	mA	1, 2, 3
		-60	—	115		
I_{CC2}	Standby Current (LVTTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		—	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min)	-50		140	mA	1, 3
		-60	—	115		
I_{CC4}	EDO (Hyper Page) Mode Current Average Power Supply Current, Hyper Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-50	—	105	mA	1, 2, 3
		-60	—	85		
I_{CC5}	Standby Current (LVCMOS)- Low Power Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	200	µA	
	Standby Current (LVCMOS)- Standard Power Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	1	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-50	—	140	mA	1, 2
		-60	—	115		
I_{CC7}	Self Refresh Current (LP version only) Average Power Supply Current during Self Refresh CBR cycle with $\overline{RAS}$ ≥ t_{RASS} (min); $\overline{CAS}$ held low; $\overline{WE}$ = V_{CC} - 0.2V; Addresses and D_{IN} = V_{CC} - 0.2V or 0.2V.		—	400	µA	
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≥ V_{IN} ≥ V_{CC}), All Other Pins Not Under Test = 0V		-2	+2	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≥ V_{OUT} ≥ V_{CC})		-2	+2	µA	
V_{OH}	Output High Level (LVTTL) Output “H” Level Voltage (I_{OUT} = -2mA)		2.4	—	V	
V_{OL}	Output Low Level (LVTTL) Output “L” Level Voltage (I_{OUT} = +2mA)		—	0.4	V	
V_{OH}	Output High Level (LVCMOS) Output “H” Level Voltage (I_{OUT} = -100µA)		V_{CC} - 0.2	—	V	4
V_{OL}	Output Low Level (LVCMOS) Output “L” Level Voltage (I_{OUT} = +100µA)		—	0.2	V	4

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Column address can be changed once or less while $\overline{RAS}$ =V_{IL} and $\overline{CAS}$ =V_{IH}.
4. V_{OL} (LVCMOS) and V_{OH} (LVCMOS) levels are not intended for use as timing reference levels. LVCMOS levels are the quiescent state of a low impedance output driver, under the specified load condition.

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AC Characteristics (T_A=0 to +70°C, V_{CC}=3.3 ± 0.3V)

1. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
2. AC measurements assume t_T=2ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Valid column addresses are only A0 through A9.

Read, Write, Read-Modify-Write and Refresh Cycle (Common Parameters)

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RC}	Random Read or Write Cycle Time	84	—	104	—	ns	1
t_{RP}	$\overline{RAS}$ Precharge Time	30	—	40	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	8	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	50	100k	60	100k	ns	1
t_{CAS}	$\overline{CAS}$ Pulse Width	8	100k	10	100k	ns	1
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	7	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	7	—	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11	37	14	45	ns	2
t_{RAD}	$\overline{RAS}$ to Col. Address Delay Time	9	25	12	30	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	8	—	10	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	40	—	50	—	ns	1
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	1
t_{OED}	$\overline{OE}$ to D_{IN} Delay Time	13	—	15	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time From D_{IN}	0	—	0	—	ns	5
t_{DZC}	$\overline{CAS}$ Delay Time From D_{IN}	0	—	0	—	ns	5
t_T	Transition Time (Rise and Fall)	1	50	1	50	ns	6

1. In a Test Mode Read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} are delayed by 5ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5ns.
2. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. Either t_{DZC} or t_{DZO} must be satisfied.
6. AC measurements assume $t_{T = 2ns.}$

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Write Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	1
t_{WCH}	Write Command Hold Time	7	—	10	—	ns	
t_{WP}	Write Command Pulse Width	7	—	10	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	8	—	10	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	8	—	10	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	2
t_{DH}	D_{IN} Hold Time	7	—	10	—	ns	2

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.), and $t_{CPWD} \geq t_{CPWD}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
2. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.

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Read Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RAC}	Access Time from $\overline{RAS}$	—	50	—	60	ns	1, 2, 3, 5
t_{CAC}	Access Time from $\overline{CAS}$	—	13	—	15	ns	1, 2, 5
t_{AA}	Access Time from Address	—	25	—	30	ns	1, 2, 5
t_{OEA}	Access Time From $\overline{OE}$	—	13	—	15	ns	1, 5
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	6
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	—	30	—	ns	1
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	5
t_{OEZ}	Output Buffer Turn-Off Delay From $\overline{OE}$	0	13	0	15	ns	7
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	13	—	15	—	ns	4
t_{OFF}	Output Buffer Turn-Off Delay	0	13	0	15	ns	7
t_{OES}	$\overline{OE}$ Setup Time Prior to $\overline{CAS}$	5	—	5	—	ns	
t_{ORD}	$\overline{OE}$ Setup Time Prior to $\overline{RAS}$ (Hidden Refresh)	0	—	0	—	ns	

1. In a Test Mode Read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} are delayed by 5ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5ns.
2. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. Measured with the specified current load and 100pF.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

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Read-Modify-Write Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RWC}	Read-Modify-Write Cycle Time	109	—	135	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	65	—	79	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	28	—	34	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	40	—	49	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	7	—	10	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.), and $t_{CPWD} \geq t_{CPWD}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

Extended Data Out (Hyper Page) Mode Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{HCAS}	$\overline{CAS}$ Pulse Width (Hyper Page Mode)	8	100K	10	10K	ns	
t_{HPC}	Hyper Page Mode Cycle Time (Read/Write)	20	—	25	—	ns	
t_{HPRWC}	Hyper Page Mode Read Modify Write Cycle Time	54	—	66	—	ns	
t_{DOH}	Data-out Hold Time from $\overline{CAS}$	5	—	5	—	ns	
t_{WHZ}	Output buffer Turn-Off Delay from $\overline{WE}$	0	10	0	10	ns	
t_{WPZ}	$\overline{WE}$ Pulse Width to Output Disable at $\overline{CAS}$ High	7	—	10	—	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	27	—	35	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	27	—	35	ns	1
t_{RASP}	Hyper Page Mode $\overline{RAS}$ Pulse Width	50	200K	60	200K	ns	
t_{OEP}	$\overline{OE}$ High Pulse Width	5	—	10	—	ns	
t_{OEHC}	$\overline{OE}$ High Hold Time from $\overline{CAS}$ High	5	—	10	—	ns	

1. Measured with the specified current load and 100pF at V_{OL} = 0.8V and V_{OH} = 2.0V.

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Self Refresh Cycle - Low Power version only

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RASS}	$\overline{RAS}$ Pulse Width During Self Refresh Cycle	100	—	100	—	µs	1
t_{RPS}	$\overline{RAS}$ Precharge Time During Self Refresh Cycle	84	—	104	—	ns	1
t_{CHS}	$\overline{CAS}$ Hold Time During Self Refresh Cycle	-50	—	-50	—	ns	1

1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
   If row addresses are being refreshed in an EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.
   If row addresses are being refreshed in any other manner (ROR- Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

Refresh Cycle

Symbol	Parameter		-50		-60		Units	Notes
			Min.	Max.	Min.	Max.		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)		5	—	5	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)		5	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)		5	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)		5	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time		5	—	5	—	ns	
t_{REF}	Refresh Period	SP version	—	64	—	64	ms	1
		LP version	—	256	—	256		

1. 8192 cycles for RAS Only Refresh; 4096 cycles for CBR Refresh.

Test Mode Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{WTS}	Test Mode $\overline{WE}$ Setup Time	5	—	10	—	ns	
t_{WTH}	Test Mode $\overline{WE}$ Hold Time	5	—	10	—	ns	

Counter Test Mode Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{CPT}	$\overline{CAS}$ Precharge Time in Counter Test Cycle	40	—	40	—	ns	

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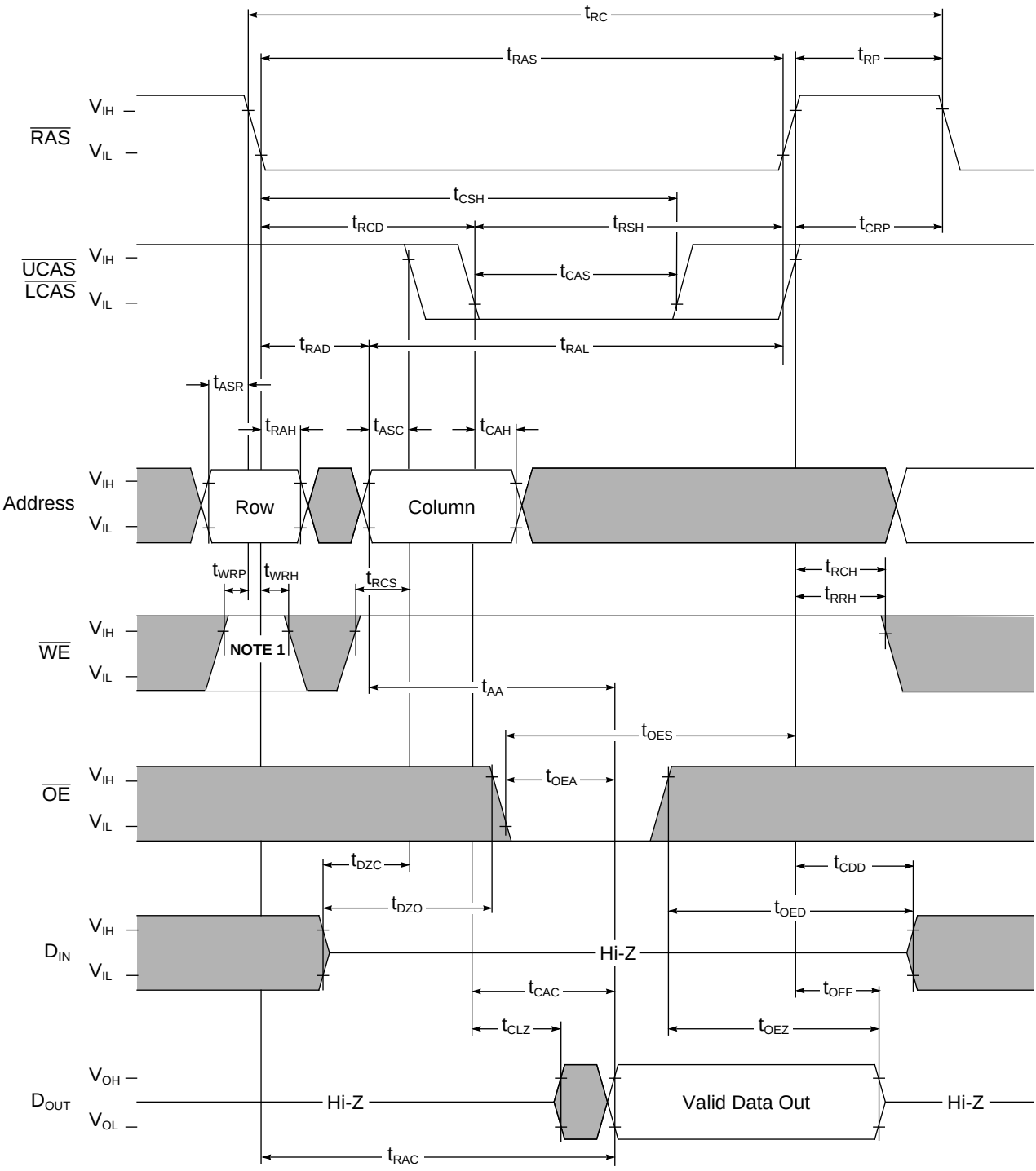
Read Cycle



: "H": or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

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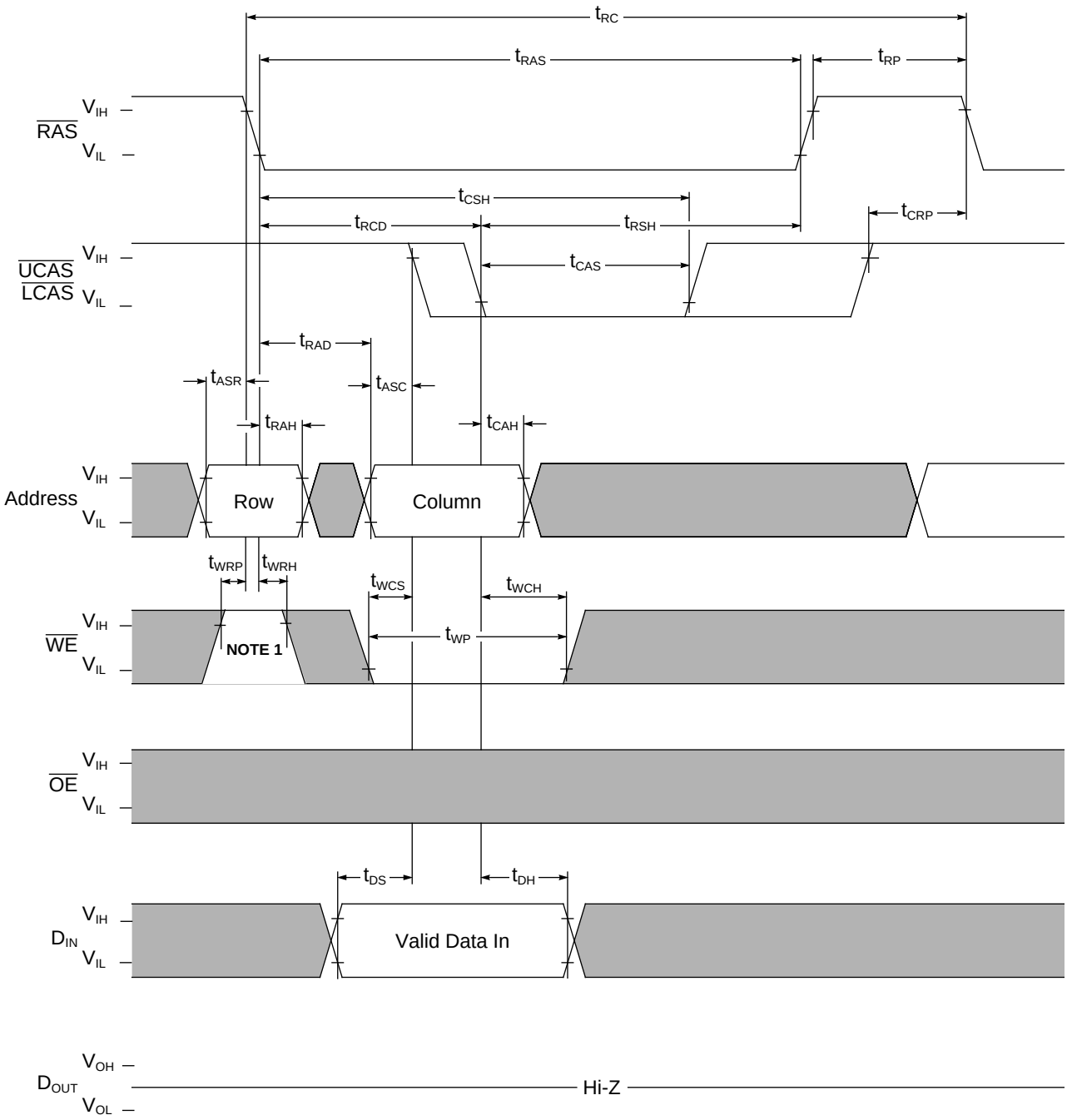
Write Cycle (Early Write)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

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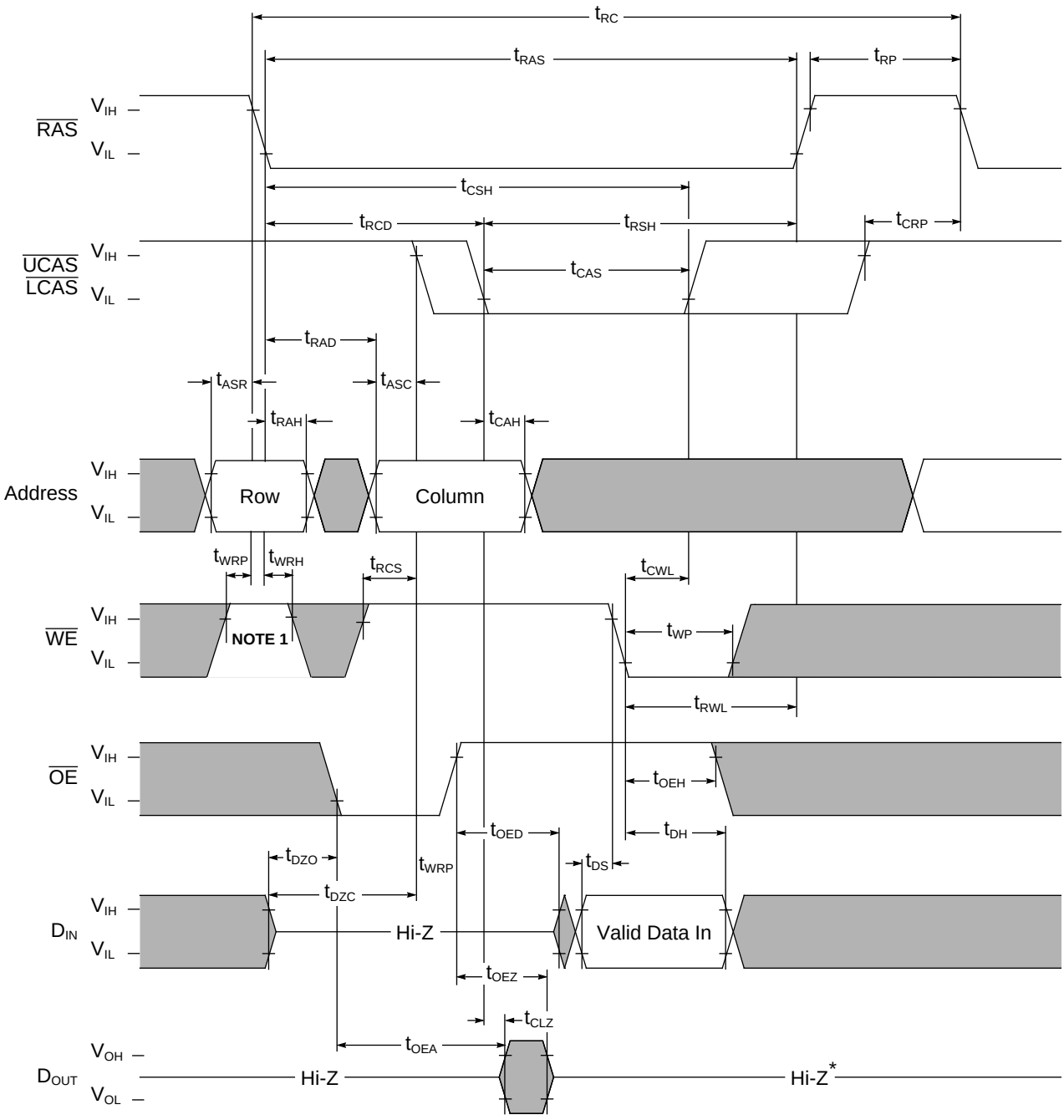
Write Cycle (Delayed Write)



: "H" or "L"

* t_{OEH} greater than or equal to t_{CWL}

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

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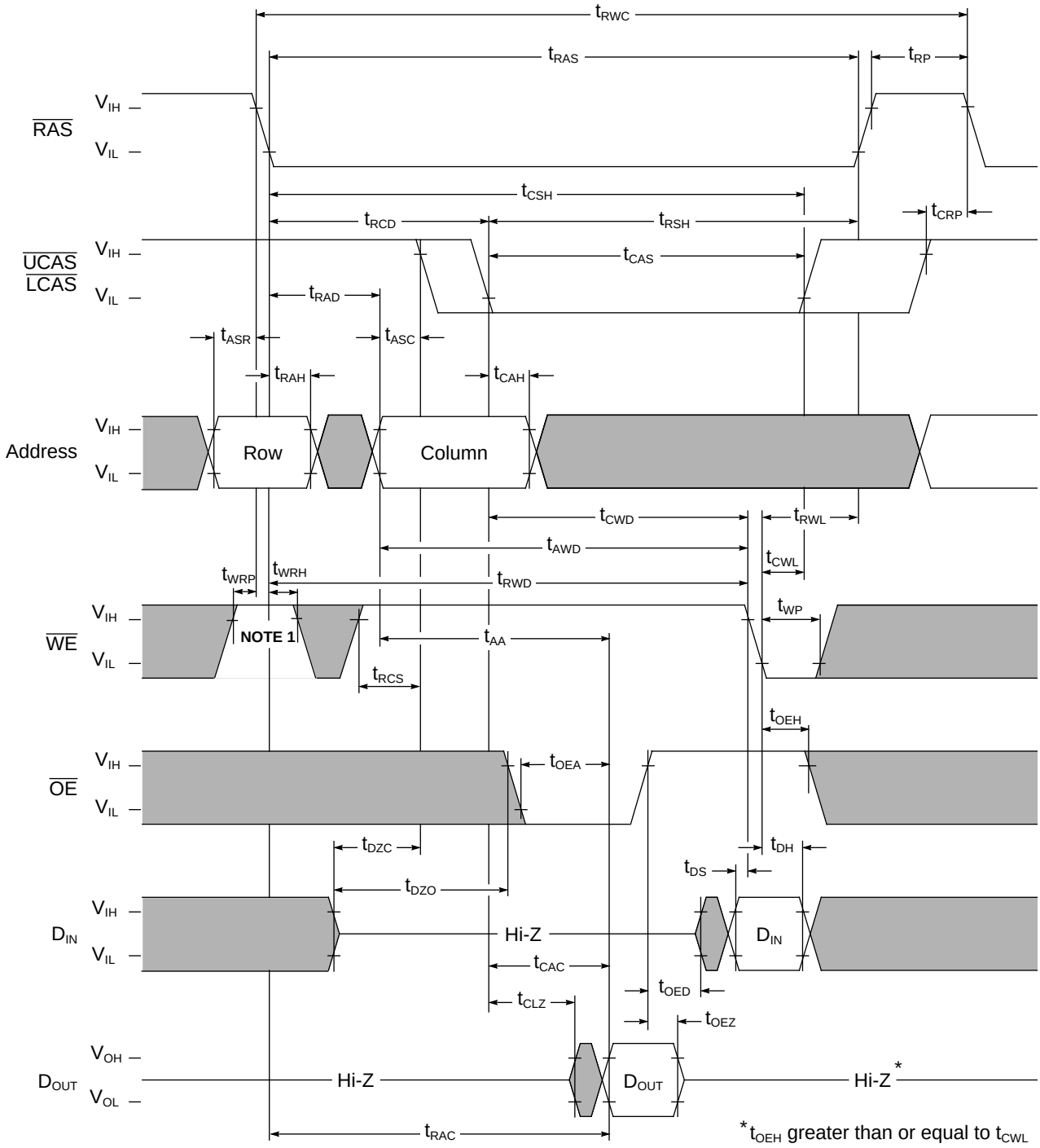
Read-Modify-Write Cycle



: “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

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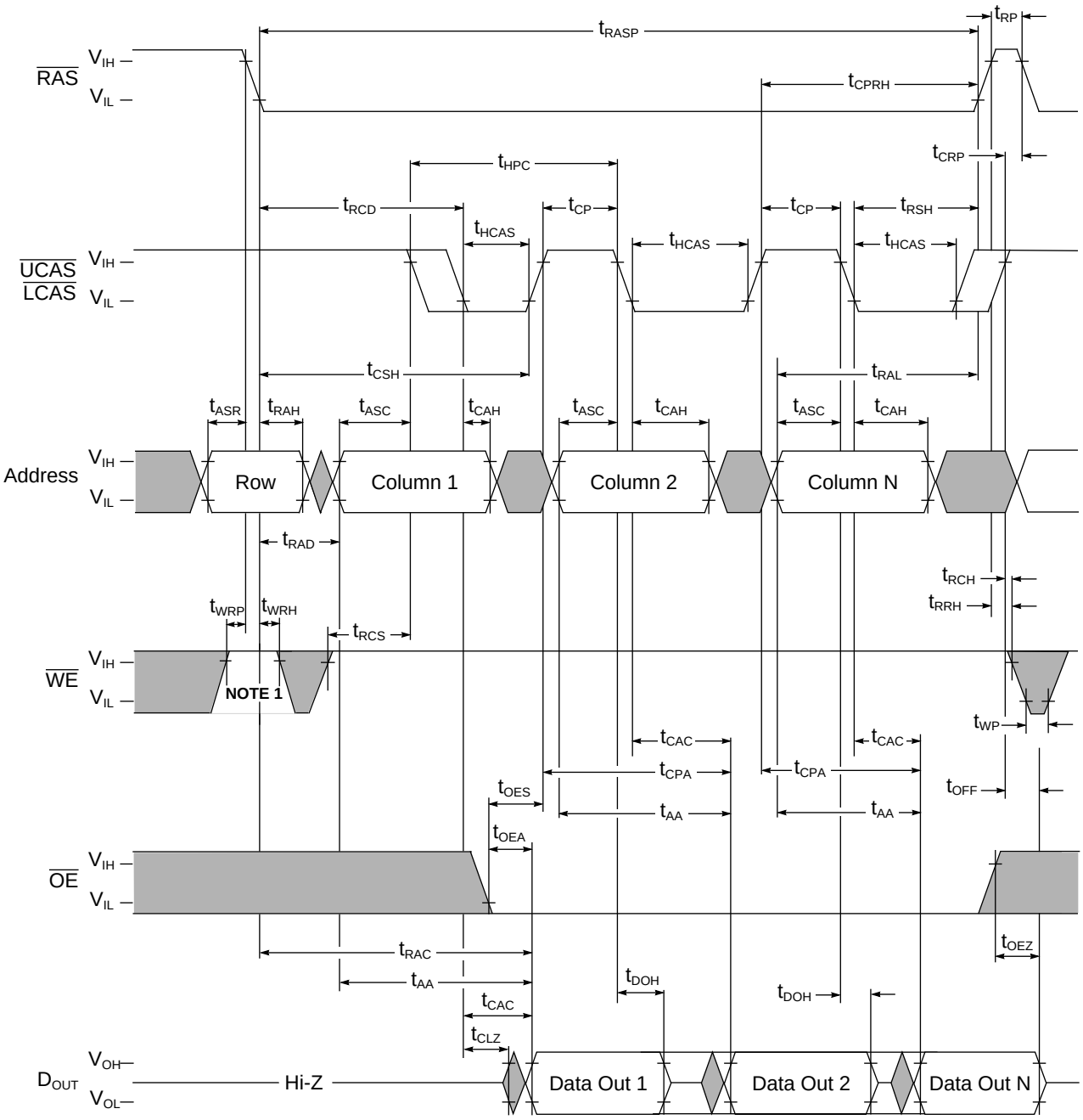
Hyper Page Mode Read Cycle



: “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

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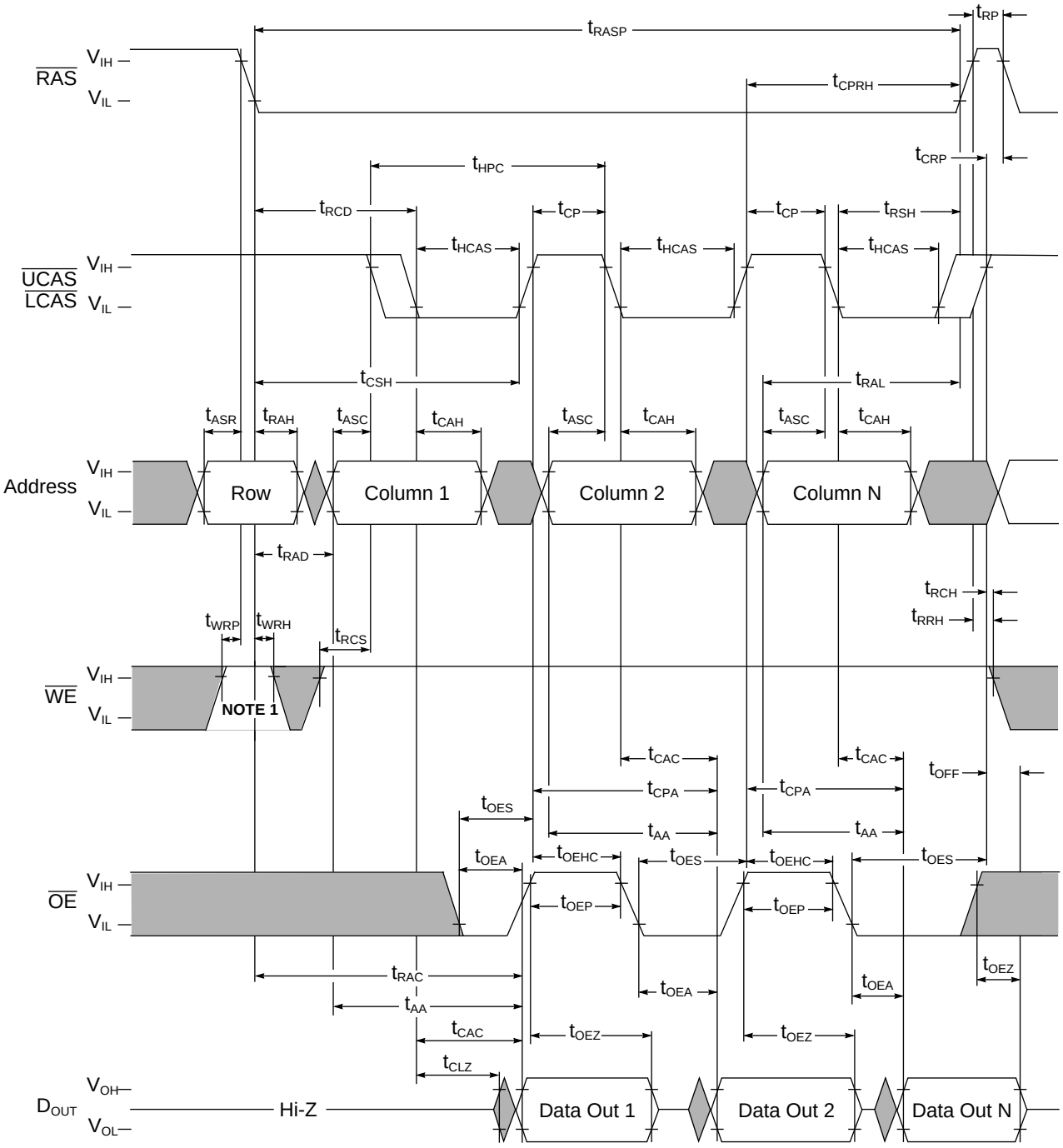
Hyper Page Mode Read Cycle ($\overline{OE}$ Control)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

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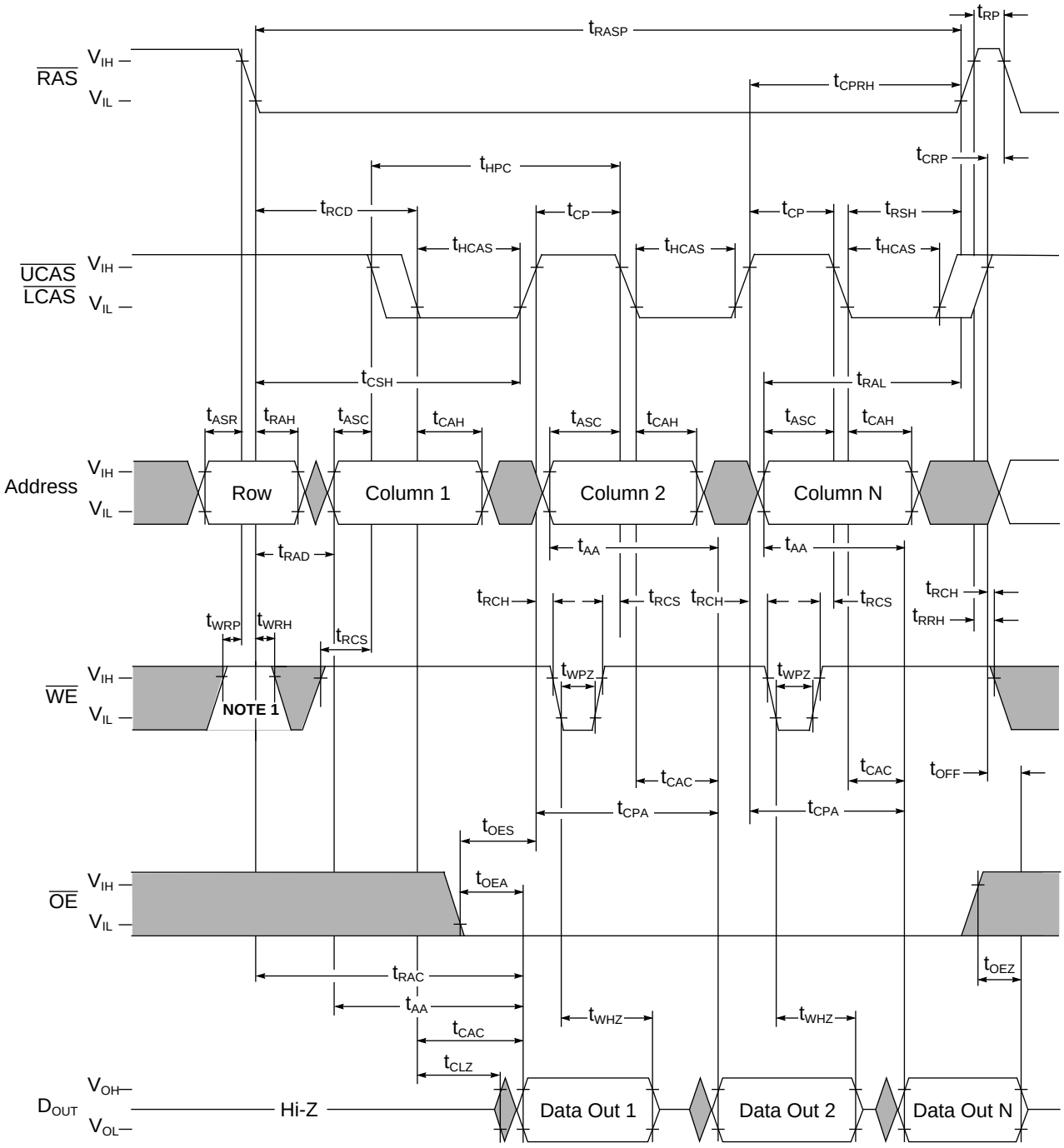
Hyper Page Mode Read Cycle ($\overline{WE}$ Control)



: “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

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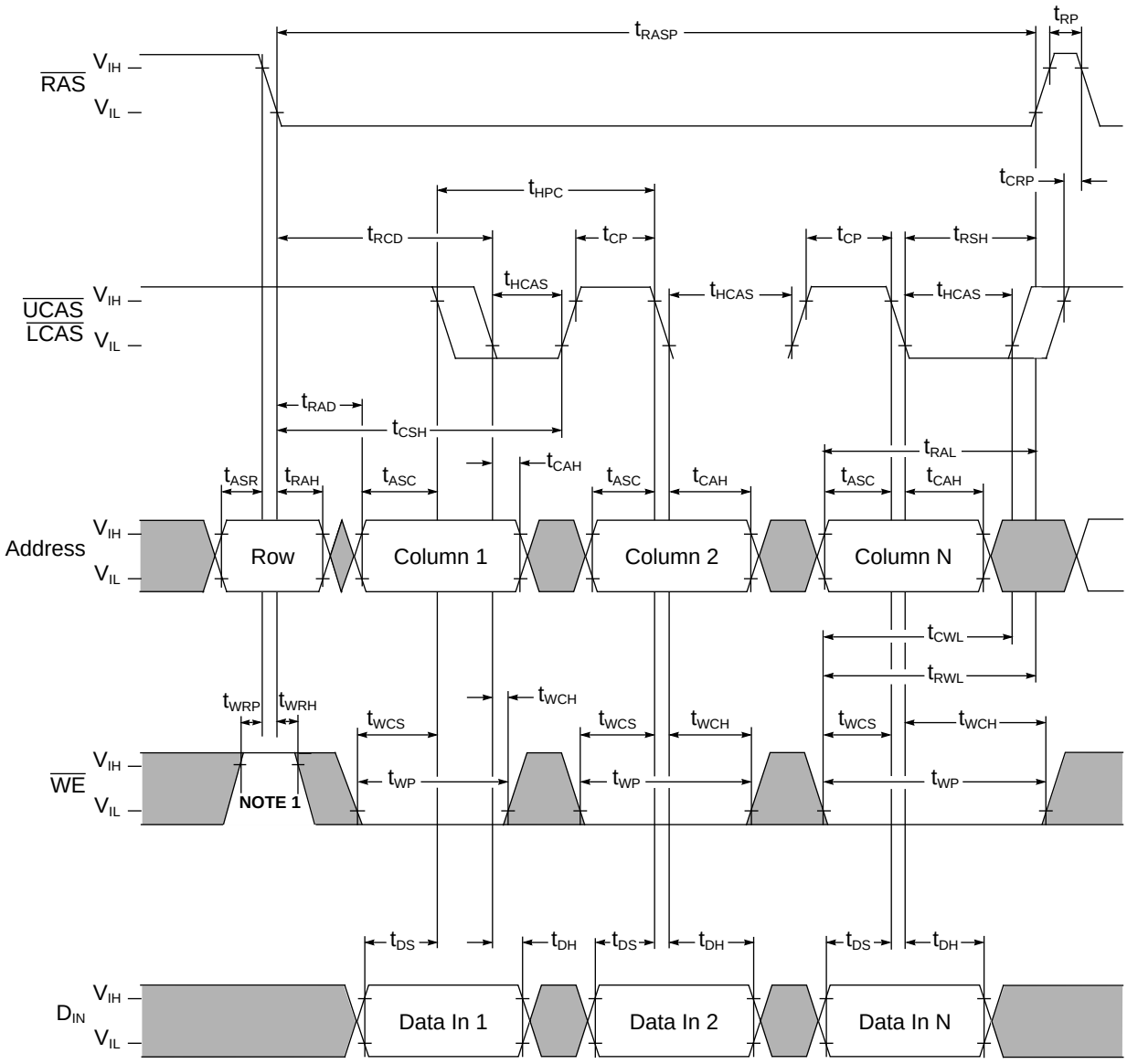
Hyper Page Mode Early Write Cycle



: “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

$\overline{OE}$ = Don’t care

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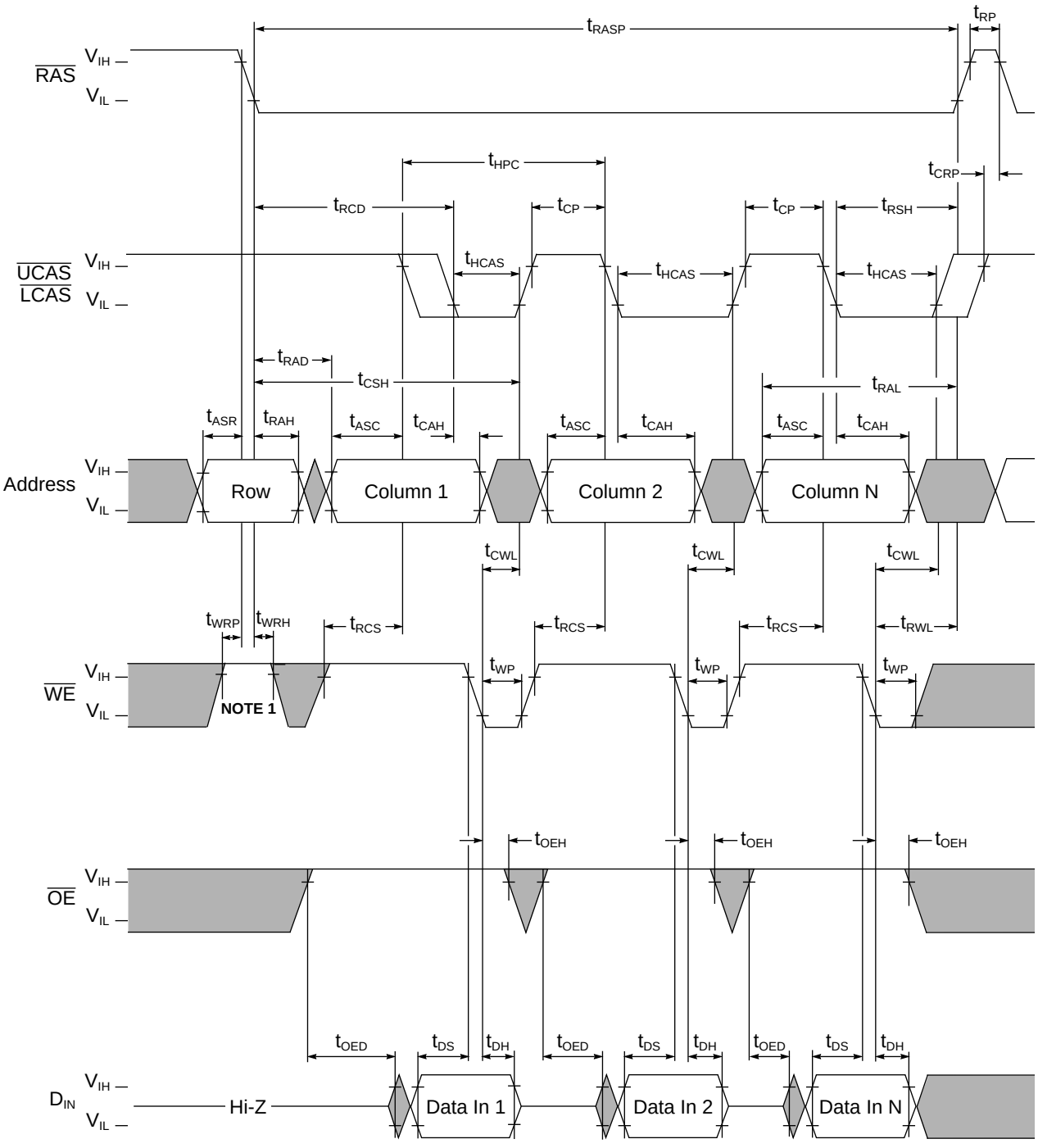
Hyper Page Mode Late Write Cycle



: “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

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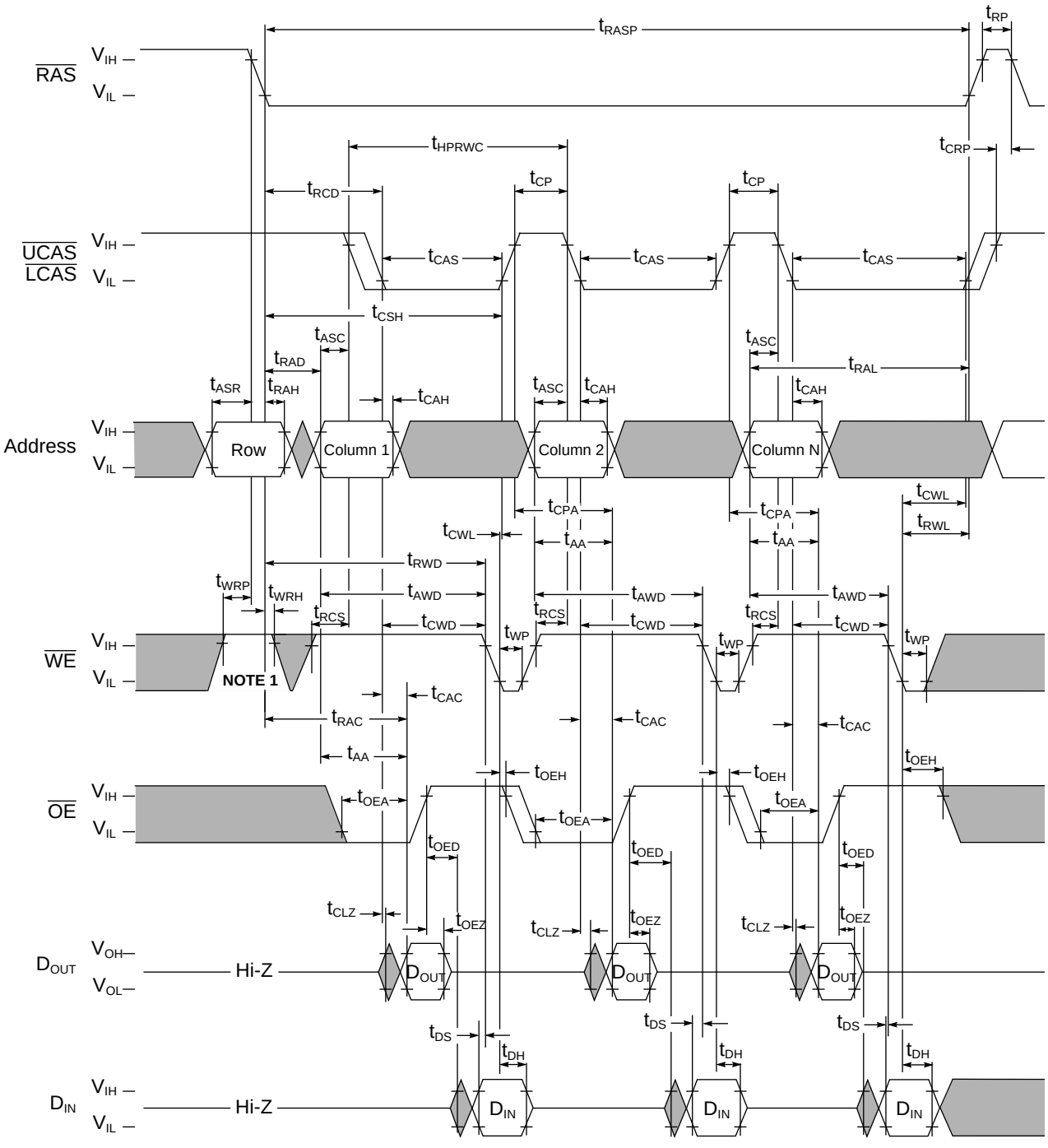
Hyper Page Mode Read Modify Write Cycle



: “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

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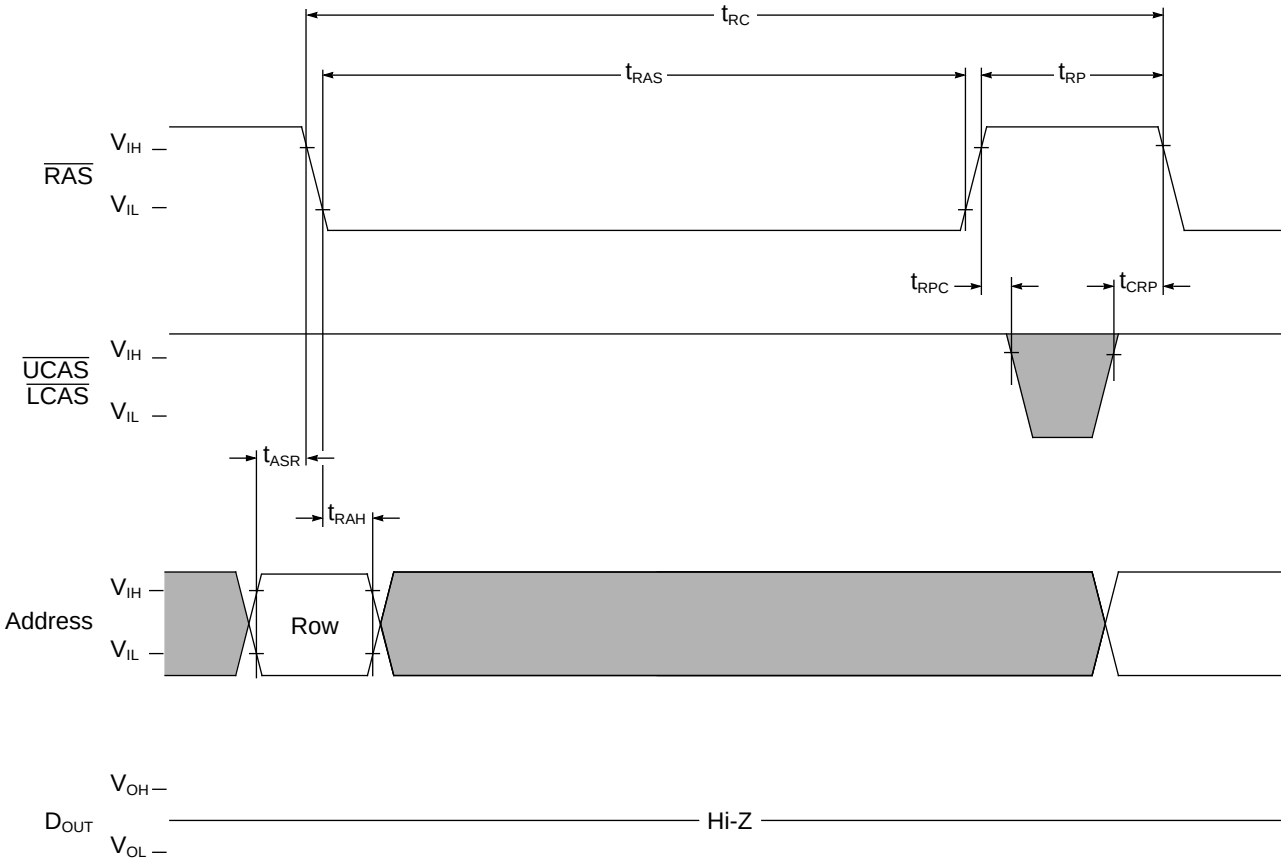
$\overline{RAS}$ Only Refresh Cycle



: “H” or “L”

NOTE: $\overline{WE}$, $\overline{OE}$ and D_{IN} are “H” or “L”

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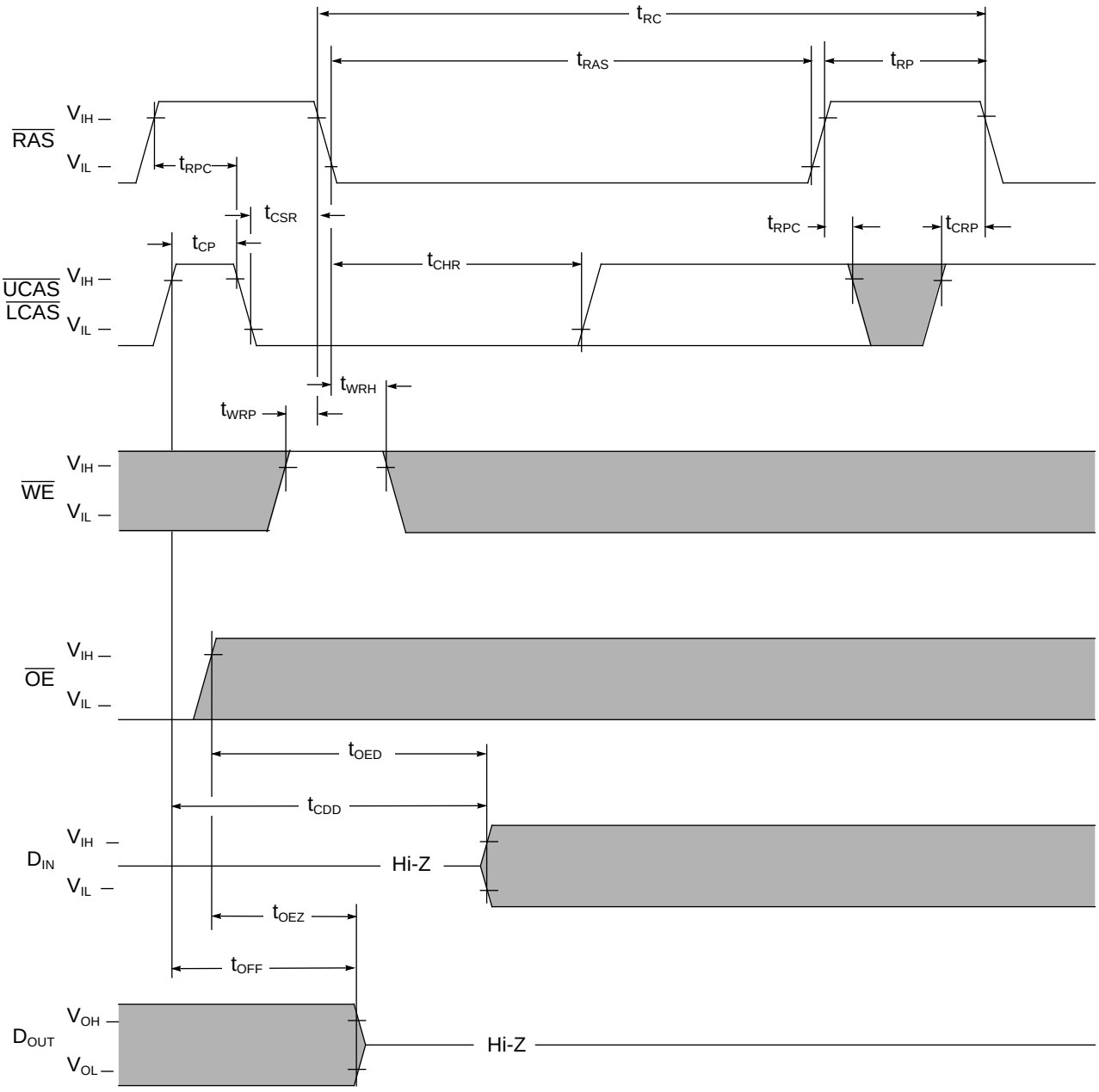
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



: “H” or “L”

NOTE: Address is “H” or “L”

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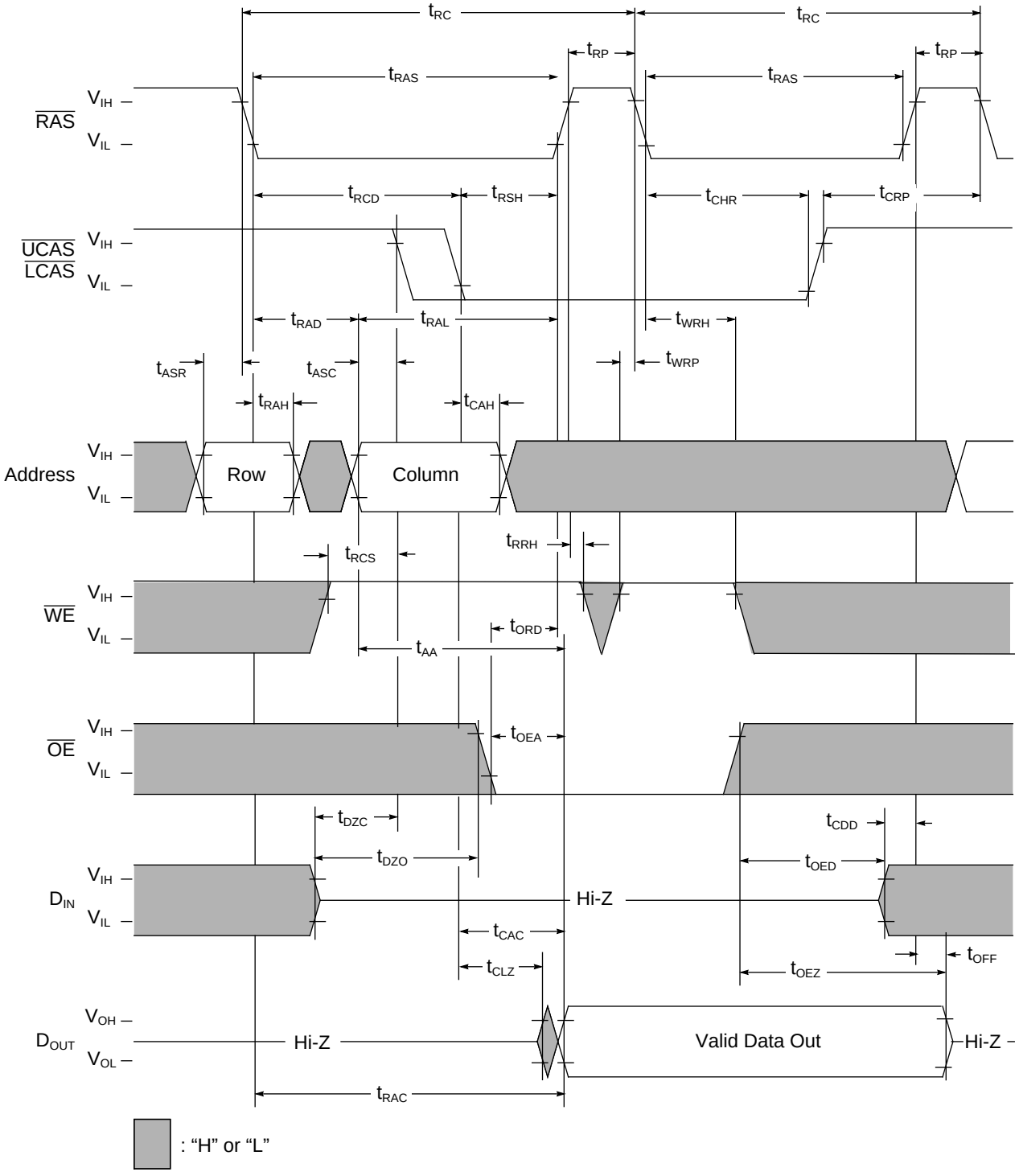
Hidden Refresh Cycle (Read)



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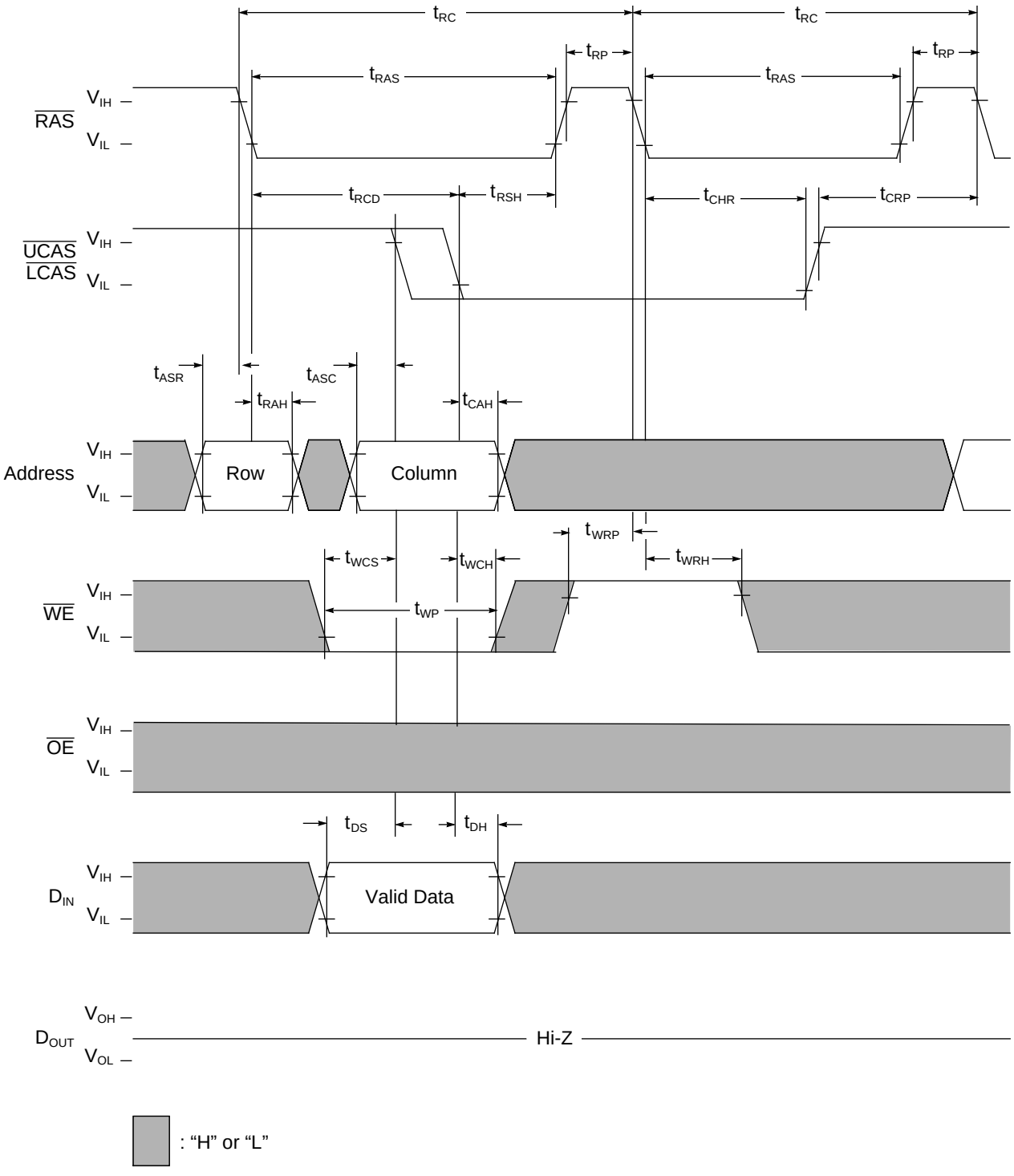
Hidden Refresh Cycle (Write)



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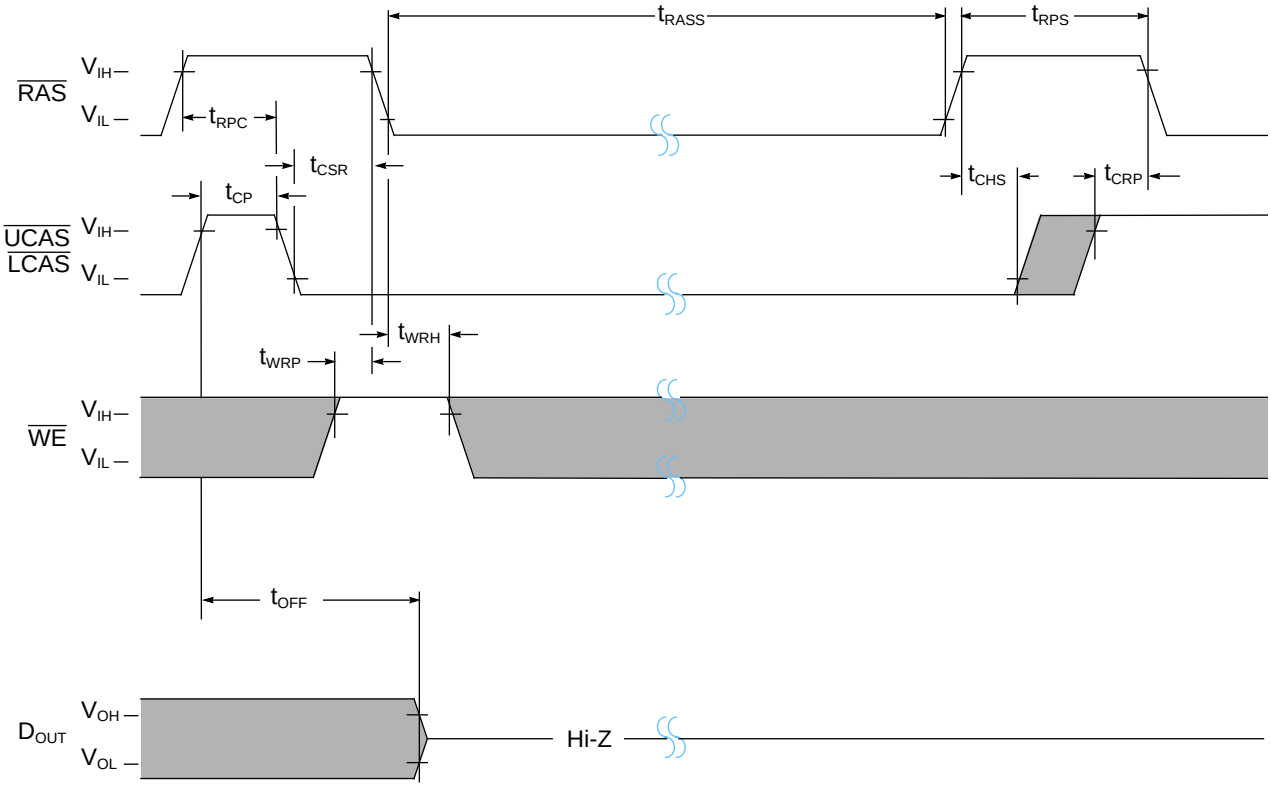
Self Refresh Cycle (Sleep Mode) - Low Power version only



: "H" or "L"

NOTE: Address and OE are "H" or "L"
Once t_{RASS} (min) is provided and RAS remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."

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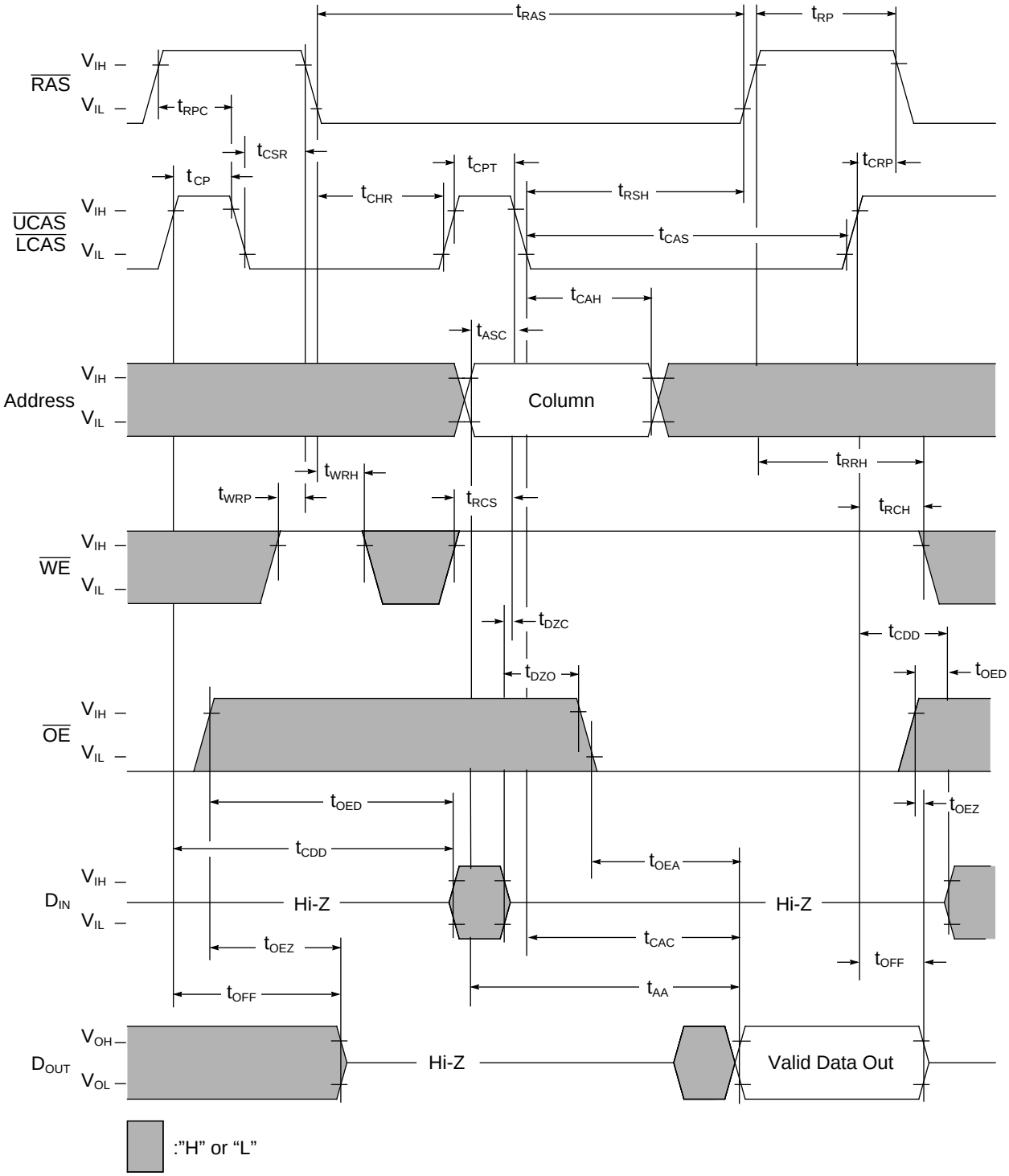
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle (Read)



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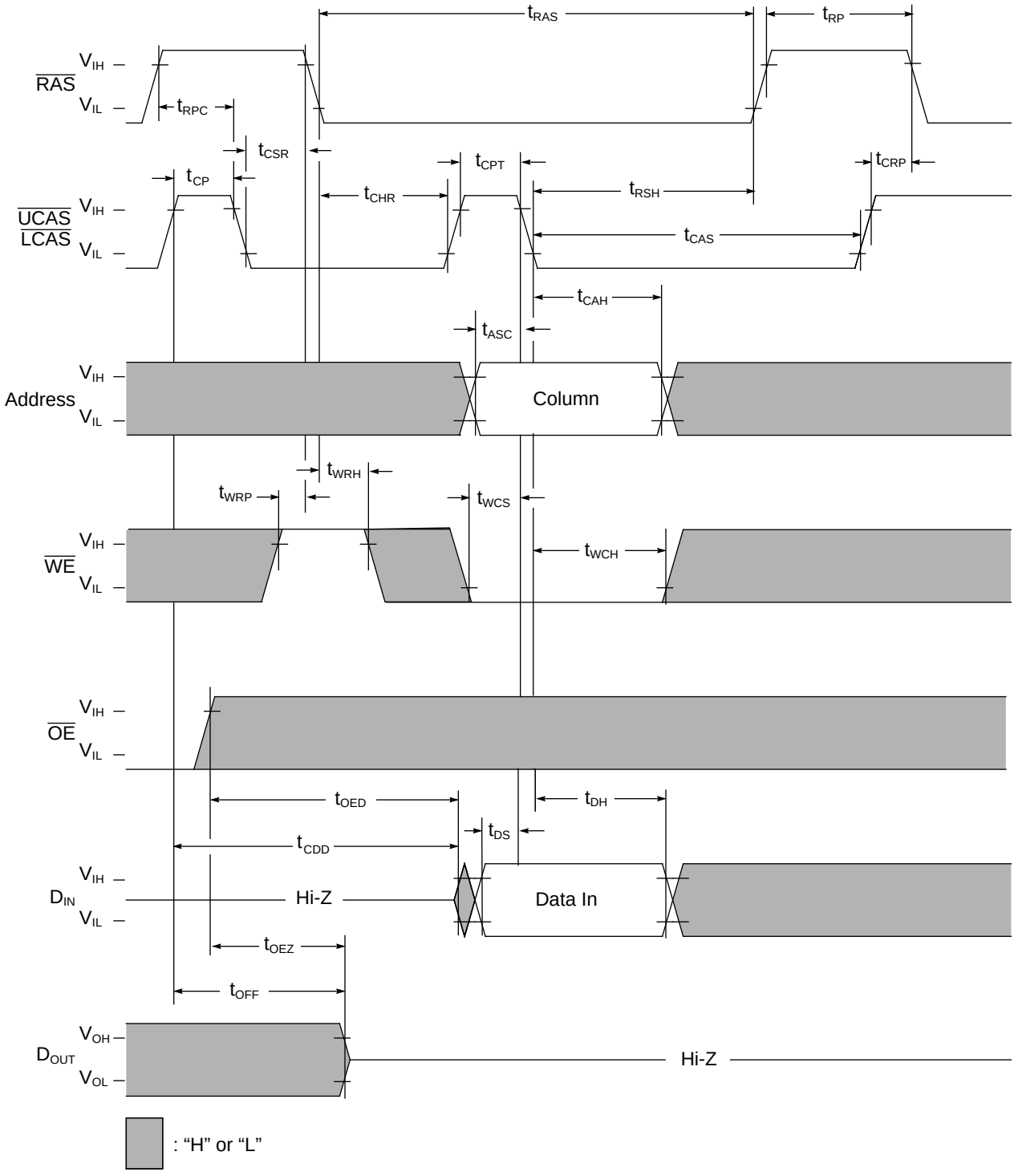
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle (Write)



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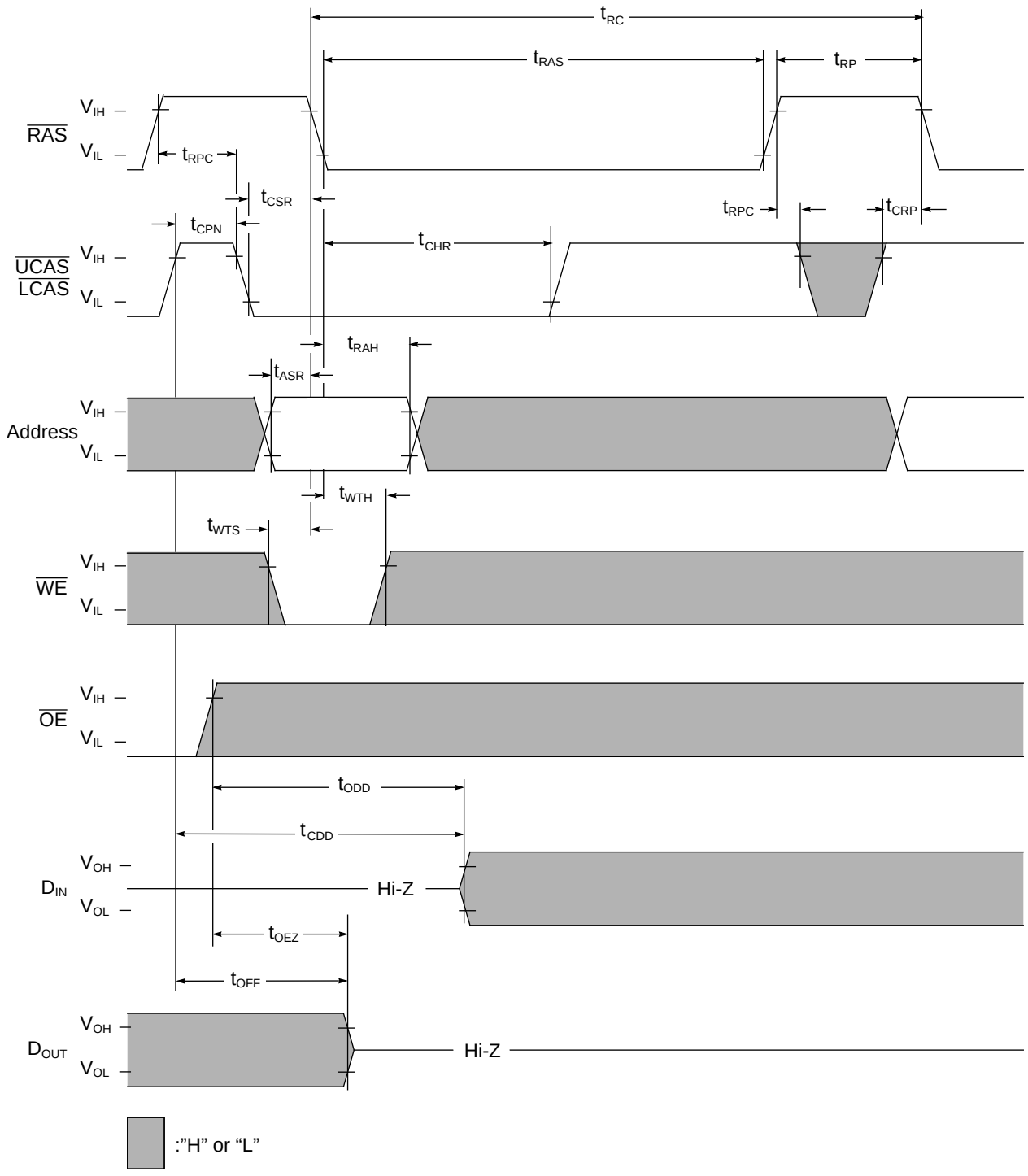
Test Mode Entry Cycle



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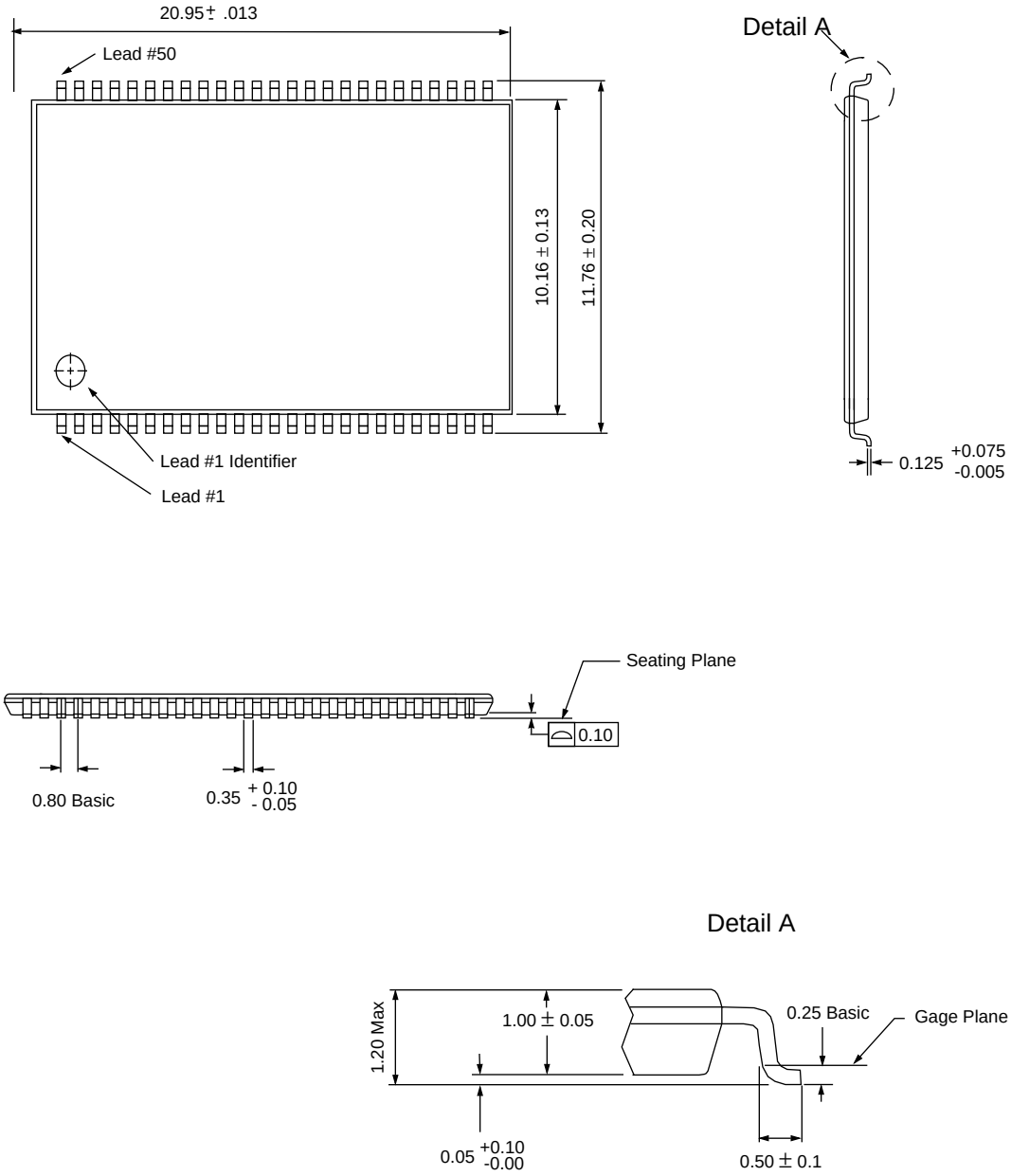
Package Dimensions (400 mil; 50 lead; Thin Small Outline Package)



NOTE: All dimensions are in millimeters. Reference JEDEC Standar MS-024

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Revision	Contents of Modification
12/19/95	Initial specification release.
04/03/96	1. $\overline{WE}$ for the Hidden Refresh Write cycle in the Truth Table was changed from “L” to “H” 2. Increased the -50 Icc1 from 165ma to 175ma 3. Increased the -50 Icc3 from 135ma to 145ma; Increased -60 Icc3 from 110ma to 120ma 4. Increased the Icc5 SP from .9ma to 1ma for -50 and -60
10/11/96	1. EC’d Specification to reflect Die Rev C; Previoue Die Rev’s will not meet this level of the specification 2. Package changed from 500mil 54 pin TSOP to 400mil 50 pin TSOP 3. Decreased Icc1 from 145ma to 115ma for -60 and from 175ma to 140 for -50 4. Decreased Icc3 from 120ma to 115ma for -60 and from 145ma to 140ma for -50 5. Decreased Icc4 from 120ma to 85ma for -60 and from 150ma to 105 for -50 6. Decreased Icc6 from 125ma to 115ma for -60 and from 150ma to 140ma for -50 5.Improved -50 timing parameters (t_{RAH}, t_{CAH}, t_{RCD}, t_{CSH}, t_{WCH}, t_{RWC}, T_{RWD}, t_{CWD}, t_{AWD}, t_{WTS}, t_{WTH}, t_{CPT}) 6. Increased t_{HPRWC} for -50 from 51ns to 54ns

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